III. Remarks

A. Allowable Subject Matter

Applicants are grateful to the Examiner for recognizing the allowable subject matter set forth in the in claim 14. Claim 14 has been canceled and rewritten in independent form as claim 29. It is submitted claim 29 is in allowable form.

B. Rejection under 35 U.S.C. § 103

1. Lien et al. (6,069,782) in view of Smith et al. (5,775,112) and U.S. Patent No. 6,268,993 to Anderson.

The Action rejects claims 13, 15-20 and 23-28 as being obvious from Lien et al. in view of Smith et al. in view of newly cited U.S. Patent No. 6,268,993 to Anderson. Reconsideration and withdrawal of this rejection are respectfully requested in view of the following arguments.

As recognized by the Examiner, independent claim 13 is directed to a circuit for electrostatic discharge (ESD) protection that includes an ESD protection circuit having a stack of cascaded NMOS transistors configured to discharge an ESD pulse. In rejecting claim 13, the Examiner recognizes that "Lien and Smith do not disclose the ESD circuit having stacked NMOS transistors as claimed" but finds that Anderson discloses an ESD protection circuit 28 "having a stack of cascaded NMOS transistors (a stack of cascaded NMOS transistors P1, P2)." The Examiner cites to the Abstract and Col. 5, Lines 9-11 for support for Anderson's teaching of the claimed stack of cascaded NMOS transistors. Reconsideration of this point is respectfully requested.

Anderson does not teach a stack of cascaded NMOS transistors but rather teaches "cascoded" transistors. (See Abstract ("The technique uses an ESD protection circuit that includes two cascode-connected clamps . . ."); Col. 5, Line 12 (stating that devices P1, P2 form a "cascoded NMOS stack")). As those in the art will recognize, "cascoded" and "cascaded" refer to completely different relationships of devices. Claim 1 requires a stack of cascaded NMOS transistors. Anderson merely shows two cascoded transistors. For at least this reason, it is submitted that the Examiner has not set forth a *prima facie* case of obviousness with respect to claim 13 or it dependent claims.

Reconsideration and withdrawal of this rejection of claim 13 and dependent claims 15-20 are respectfully requested.

Independent claim 23 is directed to a method for electrostatic discharge protection that uses an ESD protection circuit comprising a stack of cascaded NMOS transistors. For the reasons set forth above in connection with claim 13, it is submitted that the Examiner has not set forth a *prima facie* case of obviousness with respect to claim 23 or its dependent claims.

Reconsideration and withdrawal of this rejection of claim 23 and dependent claims 24-28 are respectfully requested.

2. Lien et al. in view of Smith and Anderson in further view of U.S. Patent No. 5,331,391 to Dungan et al.

The Action rejects claim 21 as being obvious from Lien et al. in view of Smith and Anderson in further view of U.S. Patent No. 5,331,391 to Dungan et al. Claim 21 depends from claim 13 and is, therefore, allowable for at least the reasons set forth above in connection therewith. Accordingly, reconsideration and withdrawal of the rejection of claim 21 are respectfully requested.

IV. Conclusion

Applicants submit that this application is in condition for allowance. Early notification to that effect is respectfully requested.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679.**

Respectfully submitted,

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